data of M bits (M≠ N);

c) a converter, arranged to convert the third parallel data into fourth parallel data of N bits;

d) an error correction unit, arranged to selectively add an error correction check code to the second parallel data and the fourth parallel data,

said error correction unit performing a common addition processing irrespectively of second parallel data and the fourth parallel data. –

-- 32. An apparatus according to claim 31, wherein said encoder encodes the first parallel data to be encoded by differential pulse code modulation.--.

-- 33. An apparatus according to claim 31, wherein the second digital information is a television signal in which a video signal and an audio signal are time-division multiplexed. --.

-- 34. An apparatus according to claim 31, wherein said error correction unit adds a predetermined data amount of error correction check code for every predetermined data amount of the second parallel data or the fourth parallel data. --.

-- 35. An apparatus according to claim 31, further comprising a recording unit, arranged to record the data processed by said error correction unit on a recording medium. --.

-- 36. An apparatus according to claim 31, wherein the second digital information has a lower bit rate than the first digital information. --.

-- 37. A digital information coding method, comprising:

selectively inputting first parallel data of N bits representing a first digital information and second parallel data N bits representing a second digital information;